UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,443	12/07/2000	Stephen J. McDonagh	04148P011	2685

7590 11/02/2004

Robert B. O'Rourke
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
JOSEPH, JAISON	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/733,443	MCDONAGH, STEPHEN J.	
	Examiner	Art Unit	
	Jaison Joseph	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Lindquist et al (US Patent 5,712,637).

Regarding claim 1, Lindquist et al teach a current source (charge pump) having an output as superposition of the current steps in opposite direction at different times (see column 6, lines 45-66)

Regarding claim 2, the limitation of claim 1, Lindquist also teaches that determining a filter output (voltage at the capacitors of 19 and 20 of figure 2) that results from the charge pump output (26 of figure 2). One ordinary skilled in the art realize that capacitors are used as filters.

Regarding claim 3, Lindquist also teaches that the reference clock edges are provided by clock 23 and clock 24 of figure 2.

Regarding claims 4 and 6, the limitation can be found in column 6, line 60-67 of Lindquist et al. Lindquist et al clearly teach that the first current step is in the positive direction and the second current step is in the negative direction.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 rejected under 35 USC 103(a) as being unpatentable over Byrd et al (US Patent 4,814,726) in view of Lindquist et al (US Patent 5,712,637).

Regarding claim 5, Byrd el at teach that a PLL having a phase detector, charge pump, loop filter, and a voltage-controlled oscillator (figure 1). Byrd et al do not teach that the charge pump output is composed of successive addition of current steps. However, Lindquist el at teaches a charge pump with output signal is a composition of current steps. It would be obvious to an ordinary skilled in the art at the time of the invention to substitute Lindquist's charge pump in Byrd's PLL to enhance the efficiency and faster response of PLL performance.

Claims 14 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindquist et al (US Patent 5,712,637) in view of Carsello et al (US Patent 5,872,819).

Regarding claims14-17 and 19, Lindquist et al is cited as explained in the above paragraph. Lindquist el at failed to teach the use of machine-readable medium having stored instructions, which are executable by digital processing system to perform all the functions of the PLL. Carsello et al teach that PLL functions can be implemented by digital processor with stored executable instructions (see column 7 line 18-20). Therefore, it would be obvious to an ordinary skilled in the art to use the digital processor to implement all the functions of the PLL because it is more flexible and efficient.

Claim 14 inherits the limitation of claim 1 further Carsello discloses that all PLL functions can be implemented in a digital signal processor.

Claim 15 inherits the limitation of claim 2 further Carsello discloses that all PLL functions can be implemented in a digital signal processor

Claim 16 inherits the limitation of claim 3 further Carsello discloses that all PLL functions can be implemented in a digital signal processor

Claim 17 inherits the limitation of claim 4 further Carsello discloses that all PLL functions can be implemented in a digital signal processor

Claim 18 recites that second current step occurs when voltage controlled oscillator output clock edge rises. It is inherent that the voltage-controlled oscillator is basic component in the PLL. The voltage controlled oscillator, which inherently included in PLL in the reference Carsello.

Claim 19 inherits the limitation of claim 6 further Carsello discloses that all PLL functions can be implemented in a digital signal processor.

Claims 7 – 13 and 20 – 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrd et al (US Patent 4,814,726) in view of Carsello et al (US Patent 5,872,819) further in view of Lindquist et al (US Patent 5,712,637).

Byrd el at is cited as explained in the above paragraph. Byrd failed to teach the use of digital signal processor to perform the functions of the PLL and a charge pump having an output as superposition of current steps in opposite direction at different times. Carsello teaches all PLL functions can be implemented by digital processor (see column 7 line 18-20). Lindquist el at teaches that a charge pump having an output as

superposition of current steps (see column 6 lines 45-66). In order for the digital processor to function as PLL, the software needs to simulate the voltage output, the current of the charge pumps, the time the filter output voltage to reach the reference voltage, and the timing of the rising of the clocks. Therefore the method of calculating of voltage output, the time the output voltage reach the reference voltage, triggering the voltage controlled oscillator output clock edge, stepping the current steps, setting the filter voltage to zero, and recalculating the filter output voltage as recited in claims 7 - 13, and 20 – 26 are inherently performed by the digital processor in order for the digital processor to function as PLL.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jaison Joseph
Patent Examiner

STEPHEN CHIN
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2600